VRIJE UNIVERSITEIT BRUSSEL

The faculty of Engineering of the Vrije Universiteit Brussel invites you to attend the public defense leading to the degree of

DOCTOR OF ENGINEERING SCIENCES

of **Lucas Moura Santana**

The public defense will take place on **Friday 29th March 2024 at 4:00 pm** in room **D.2.01** (Building D, VUB Main Campus)

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TOWARDS UNCHARTED TERRITORIES: HIGH-PERFORMANCE AND HIGH-BANDWIDTH RINGAMP-BASED DELTA-SIGMA ADCs

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Abstract of the PhD research

Analog-to-digital (ADC) research often happens in an agnostic detachment from the intended application; although motivation is sometimes presented, it is not always implemented with the proposed prototype. Advancements in ADC linearity and speed enable applications that were nonexistent before to emerge, such as direct RF conversion and 8k camera recording. Most ADC architectures cover all regions of the performance space, being at the forefront of the state-of-the-art for some areas and not so much for others. This high coverage enables the use of the advantages and peculiarities of different architectures across different applications. One notable architecture that does not perform this is the Discrete Time (DT) Delta-Sigma Modulator (DSM) ADC, in which the published state-of-the-art bandwidth front is limited to 20 MHz. This work investigates this limitation, showing that it can be overcome with high-efficiency ring amplifiers (ringamps) and the correct design process. This work presents a prototype for a single loop 3rd-order DT DSM ADC based on ringamps for the loop filter that could double the bandwidth reached by DT DSM ADC at 47.5 MHz and achieve 67 dB of signal-to-noise and distortion ratio (SNDR) when clocked at 950 MHz. It also shows outstanding figures of merit (FoM): the Schreier FoM, FoMs is 167 dB and the Walden FoM, FoMw is 27 fJ per conversion step. The second prototype used time interleaving to improve the sampling rate and bandwidth further and used a noise-coupled (NC) noiseshaping (NS) SAR quantizer to enable aliased noise suppression. It achieved 1.4 GS/s of sampling rate, a decimated bandwidth of 70 MHz at a peak SNDR of 67 dB, with a power consumption of 32 mW; this translated to a FoMs of 160 dB and a FoMw of 143 fJ/c.s. Both prototypes were the first to pave the way to increase the bandwidth in DT DSM ADC efficiently and can still benefit from recent developments in ringamps and noise-shaping SAR ADCs, leading the architecture to conquer even more space in this uncharted territory.